IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Yeshwanth Narendar et al.		
Title:	METHOD FOR TREATING SEMICONDUCTOR PROCESSING COMPONENTS AND COMPONENTS FORMED THEREBY		
App. No.:	10/824,329	Filed:	April 14, 2004
Examiner:	Julio J. Maldonado	Group Art Unit:	2823
Customer No.:	34456	Confirmation No.:	5396
Atty. Dkt. No.:	1035-E4371		

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DECLARATION UNDER 37 C.F.R. §1.132

Sir, I hereby declare and state:

1. I am a joint inventor of the subject matter presently claimed in the above-identified patent application.

2. I received my PhD degree in Materials Science and Engineering from Pennsylvania State University, University Park, PA.

3. I have been employed by Saint-Gobain Ceramics and Plastics, Inc. since November 1996, wherein I have been mainly engaged in research and development of advanced ceramic materials and processes for forming same, and in particular including silicon carbide-based ceramics for use in semiconductor fabrication environments.

4. I have reviewed the Office Action dated April 20, 2007, including the positions taken by the PTO with respect to several prior art references. I have also particularly reviewed the subject matter of US 6,227,194 (Thilderkvist) and US

2003/0198749 (Kumar). For the reasons discussed below, the prior art referen es fail to disclose (or suggest) all features of the claimed invention.

5. Claimed Invention. The claimed invention is drawn to a semicondu or processing component comprising SiC, having an outer surface portion that co ists essentially of a CVD-SiC, and has a surface impurity level of not greater than 2 C the bulk impurity level (measured at a depth at least 3 microns from the outer surfa e). The notably reduced surface impurity level may be achieved through processing as escribed in the present specification, in which an outer target portion of the CVD-SiC cc ting is removed, generally through an oxidation and etch process. Typically, several c idation and etch procedures are carried out, thereby removing an outer portion of the C 'D-SiC layer that is impurity-enriched such that the outer surface portion has the claim l surface impurity level.

6. The Prior Art. The PTO relies upon Thilderkvist et al. for alleged di closure of most of the features of the claimed invention, and on the secondary reference to Kumar et al. for disclosure of CVD-SiC layer. However, the references do not even re otely suggest impurity reduction at the outer surface of the outer surface portion to th extent claimed, and further, do not even remotely *enable* such profound impurity redu ion at the outer surface. More specifically, the prior art teaches a process in which im urity reduction is carried out by coating an SiC semiconductor processing componen with a sacrificial layer that includes silicon. During coating, contaminants on or in the urface of the component are collected by the silicon-containing layer. That layer is the removed along with collected contaminants. See the paragraph bridging colum s 3 and 4 of Thilderkvist et al. We have discovered that such use of sacrificial layers to c llect or "getter" contaminants from an outer surface of an SiC component cannot achie the level of impurity reduction of the claimed invention.

More specifically, Thilderkvist et al. disclose that the process of coating t an elevated temperature can take place for a time period greater than about 50 sec, uch as 85 sec or 120 sec and that multiple coating an removing cycles may be performe l, such as 2 to 10 cycles (see column 6, lines 13-15 and column 9, line 66 to column 10 line 34).

The temperature range for high temperature treatment is about 1000°C to 1100° C, as taught in the foregoing text. 7. Testing of the Prior Art. Provided below are data that I collected to illustrate the degree to which the sacrificial (gettering) layer of the prior art is

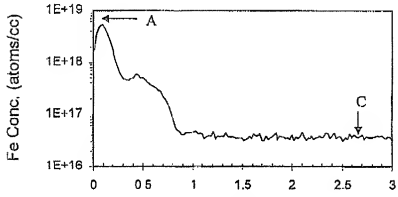

FIG. 1

effective to purify a surface portion of a CVD-SiC layer of a semiconductor processing component.

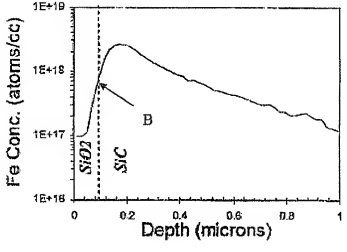

FIG. 2

FIGs. 1 and 2 illustrate impurity concentration (Fe concentration) in ato s/cc as a function of depth of an SiC layer formed by CVD. As shown in FIG. 1, the out surface portion in the first micron of depth has a notably elevated iron concentration, st olilizing at a background level or bulk impurity level at a depth below 1 micron. FIG. 2 nows the first micron in more detail.

The semiconductor processing component carrying the CVD-SiC coatin was processed to form a 1500 Angstrom silicon-containing sacrificial layer in order getter (collect) contaminants from the CVD-SiC layer, shown in FIG. 2. The sacrifici l layer and CVD-SiC layer were then subjected to high temperature annealing at 1200° in an atmosphere containing Ar and H_2 to effect purification. The high temperature a nealing treatment was continued for 12 hours in order to drive contaminants into the sac ificial layer After the 12 hour treatment, the sacrificial layer was removed and iron ir purity levels were measured. Three notable impurity levels were measured, including he original surface impurity level A at the SiC surface, post-treatment surface impu ity level B at the SiC surface, and bulk impurity level C at a depth of 3 microns, as illust ated in Figs 1 and 2 from the measurements.

8. Observations and Conclusion. The parameters were chosen to not or y faithfully recreate the prior art, but to simulate extreme purification relative to t e teachings of Thilderkvist. Thilderkvist teaches up to 120 seconds, 1100°C treat ient, which can be repeated up to 10 times. The treatment protocol herein was carrie out at an even higher temperature (1200°C) to drive further impurity migration and pu ification; and the 12 hour treatment is equivalent to 360 cycles, well beyond the 2-10 cyc s of the prior art Still, while it was shown that the sacrificial layer was effective to redu ce impurity levels a full order of magnitude from 5E18 atoms/cc (original surface i npurity level A at the SiC surface) to 7E17 atoms/cc (post-treatment surface impurity le el B at the SiC surface), it is quite clear that the thus purified outer surface portion still s quite dirty, having an impurity level of 20X the bulk impurity level of 3.5E16 (Level ').

In contrast, the claimed invention specifically calls for a surface impurit level not greater than 2X the bulk impurity level. The use of a sacrificial layer enabl l only

moderate reduction in impurity level not even remotely close to 2X that of the bulk impurity level (about 7E16 atoms/cc). That is, the claimed invention provides a minimum of a full order of a magnitude purer surface than the prior art, the Thilderkvist/Kumar combination.

The reason for the limited effectiveness of use of a sacrificial gettering layer is actually quite clear to me. As is shown, the concentration of impurities extends to a depth of about 1 micron. Due to the low diffusion coefficient of impurities in SiO2, the ability to purify through use of a sacrificial gettering layer is limited to about 25 nm. Accordingly, the use of a sacrificial gettering layer of the prior art cannot effectively clean the outer surface portion to an impurity level as claimed.

I have demonstrated that the approach taken by the prior art, which focuses on use of a silicon-containing sacrificial gettering layer, cannot enable impurity reduction to a level on the order of the claimed invention. I acknowledge that the PTO has taken a position that improved purity of the Thilderkvist/Kumar combination would have been obvious, as being a matter of routine experimentation. However, this is not the case, as the gettering technology of Thilderkvist/Kumar is ineffective to achieve the claimed purity levels. It is again noted that the claimed invention was developed based not on gettering technology, but an iterative oxidation/etch technology.

8. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like, so made, are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Respectfully submitted,

6/30/08
Date

Yeshwanth Narendar